

Figure 1: Allwinner Nezza D1 Board [1]

## Introduction & Background

- Xinu is an Educational/Research operating system (OS)
- It runs on bare-metal platforms as opposed to virtual systems
- It is taught in many Universities across the world
- Bare-metal teaching had advantages that can deepen student understanding

As architecture and operating systems evolve it is important to keep our educational tools up to date with ports and expansions aimed at improving educational outcomes.

## The Problem

### Motivations to switch to RISC-V architecture:

- Easy memory protection
- Simplified privilege scheme
- Highly intentional interrupt schemes
- Top-down design

### Problems with current implementation:

- The security of RISC-V's new protection model was thwarted
- The modified bootloader was left in a fragile state, easily broken by future updates
- Memory protection dysfunctional

## References

[1] AWOL. "D1-H Development Board — Nezza." AWOL Documentation. [https://docs.awol.com/d1/en/d1\\_dev/](https://docs.awol.com/d1/en/d1_dev/)

[2] Pillai, Vysakh P. "Exploring Virtualization in RISC-V Machines." embeddedinn. May 30, 2021. [https://www.embeddedinn.com/articles/tutorial/exploring\\_virtualization\\_in\\_riscv\\_machines/](https://www.embeddedinn.com/articles/tutorial/exploring_virtualization_in_riscv_machines/)

## The Bootloader

### Prior work was left with some issues:

- Modified U-Boot image caused:
  - Mid initialization crash
  - Incorrect launch of the kernel in M-mode
  - Un-maintainable version dependency
- Default U-Boot utilized unnecessary hardware features that bloated the image and booting process

### To address these issues, we:

- Rebuilt U-Boot image from scratch
- Implemented custom U-Boot SPL assembly code

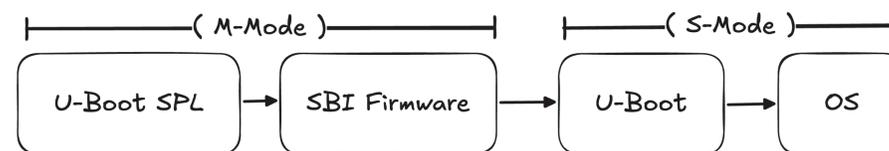


Figure 2: U-Boot Boot Process on RISC-V

## The Kernel

### With the bootloader working to specification, the following changes were made to the kernel:

- Assembly commands utilized S-mode counterparts
- M-mode control flow now nestled entirely in S-mode
- Interrupt control preserves configuration
- Timer interrupts changed to be cyclic

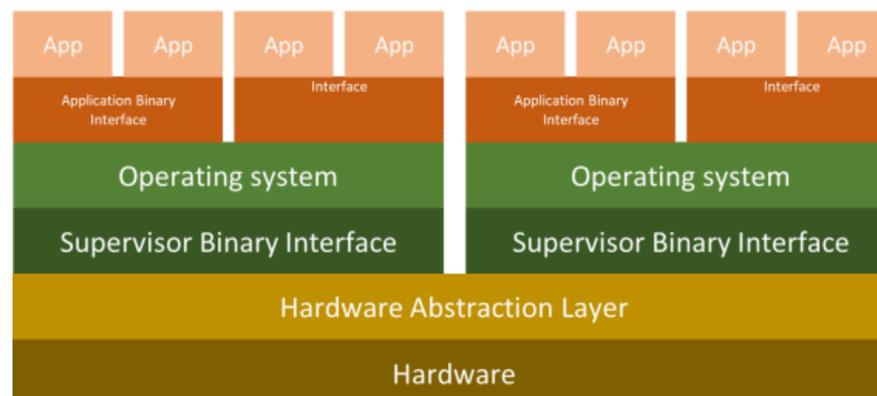


Figure 3: RISC-V Privilege Level Scheme Diagram [2]

## Results

### With the changes made during research, RISC-V Xinu matches specification with improved booting. This provides:

- A simpler control flow between privilege modes
  - Allowing students an easier conception of this complicated topic
- A stable bootloader configuration with:
  - Reduced boot times (~20 sec)
  - Stable & hardcoded MAC addresses
  - Reduced need for firmware maintenance
- Kernel works to RISC-V specification
- Kernel independent of M-mode
- Eliminated most timer skew

## Future Work

### Completing this work opens the door for research and course assignments in the following areas:

- Atomic operations & locking
- Messaging & system buffers
- Timekeeping & preemption
- Asynchronous operations

### Projects students could get hands on experience with:

- Asynchronous serial port drivers
  - Using buffers, semaphores & interrupt control
- The Xinu shell
  - Using Async serial ports and processes
- Pseudo Filesystem I/O
  - Using 2<sup>nd</sup> serial port & above additions

Changes are currently live in Marquette's Operating Systems Course, with 70 students. Differences in academic performance will be measured at the end of Spring Semester 2026.